

## 01-222N(F) -- NEXT GENERATION CHARGED-PARTICLE ARRAY DEVELOPMENT

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**Purpose:** Since the early 1990s in the field of low energy nuclear science there has been worldwide interest in an advanced facility capable of producing energetic, high-quality beams of radionuclides. The purpose of this LDRD project is to develop design concepts for the major components of the Rare Isotope Accelerator (RIA). This project aims to develop a fast high-granularity detector array to enable the next generation of experiments that will be possible with RIA.

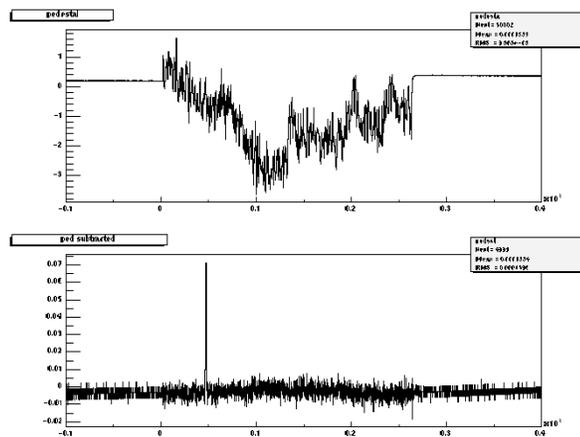
**Approach:** The physics to be performed with RIA involves experiments with very weak beams and small cross-sections. A significant effort on the detection of the signals in such experiments is warranted. A model detector array has been studied to quantify the requirements for such a system.

**Technical Progress and Results:** The requirements and technical specifications for the detector elements needed for a next generation, charged-particle-detector array are guided by a prototypical design consisting of 100 double-sided, position-sensitive strip detector elements. Each element consists of 64 position sensitive strips with double-ended readout on one side, and ordinary strips on the other side. Thus, there is a total of 192 channels per detector element, and a total number of channels of 19200 for a 100-element device. One promising candidate for the front-end stage of the read-out electronics is the VA-HDR family of ASICs (Application Specific Integrated Circuits) that contains up to 128 channels of FET preamplifier, signal shaping and multiplexed readout in a single integrated circuit chip. These chips are available in a variety of dynamic ranges, shaping time ranges, and noise/detector capacitance characteristics. Particularly attractive are the VA-HDR3 and VA-HDR6 chips, which can accept energy signals of 50 MeV or more, with a nominal base energy resolution of only a few keV (the ultimate noise response will be dominated by the silicon sensor itself). One additional advantage of these chips is that their readout can be made sequential, so that a series of chips can be read out, thereby trading off the cost of digitizing circuitry with the time of readout (typically 0.5  $\mu$ sec/channel).

For evaluation purposes, we have obtained a number of silicon pad detectors mated to the VA-HDR2 chip. These were read out using chip control electronics obtained from

CERN, coupled with National Instruments digitizers. Signals were also analyzed with a LeCroy model 9374 Digital Oscilloscope. The detectors have one side divided into a set of 120 pads, each of which is connected to one channel of the HDR2 chip. The remaining 8 channels of the HDR chip are connected to evaluation structures on the detector. Figure 1 illustrates the principle of operation of these chips. Figure 1a displays the average pedestal behavior for a string of four 128 channel chips, with the quiescent pedestal signal plotted as a function of the readout time. The clock time per channel is 500 nsec. Figure 1b shows a typical, pedestal-subtracted, output pulse train for an event with an electron hit in one pad of one of the four detectors in the string (the spike at readout time  $t \sim 50 \mu\text{sec}$ .) For each event the entire pulse train is digitized, pedestals subtracted, and the signals associated with the readout pad by their position in the pulse train. For example, the spike in Figure 1b occurs at  $t = 50 \mu\text{sec}$ . With a clocking frequency of 2MHz, or  $.5 \mu\text{sec}$  per channel, the signal seen in Figure 1b implies that one is dealing with an event with a particle in pad 100 of the first sensor in the string.

Figure 1. (a) Pedestal values plotted versus readout time for four 128-channel VA-HDR chips in series, each affixed to a silicon pad detector. (b) Pedestal-subtracted pulse train for an event with one electron depositing charge in one pad of the first of the four pad detectors (spike near readout time  $T = 50 \mu\text{sec}$ ).



Source tests. Some results of our detector evaluations appear in Figures 2 and 3 which present conversion-electron and  $\alpha$ -particle energy spectra obtained using the silicon-pad detectors described above. Figure 2 presents conversion-electron spectra from (a)  $^{57}\text{Co}$  and (b)  $^{113}\text{Sn}$  conversion electron sources with respective electron energies of 114 keV and 363 keV. The resolution of the signals is approximately 15-20 keV FWHM in each case. Contributions to the resolution include the effects of energy loss in the inactive layers of the silicon pad detectors, and noise from the electronics. While the resolution in this case is somewhat poorer than ideal for conversion electron spectroscopy, other chip versions with a more restricted dynamic range would likely perform well for that application.

Figure 2. Conversion-electron energy spectra measured with a silicon pad detector read out with the VA-HDR2 chip. (a) Electrons from  $^{57}\text{Co}$  with  $E(e^-)=114$  keV. (b) Electrons from  $^{113}\text{Sn}$  with  $E(e^-)=363$  keV. The curves are Gaussian fits to the peaks to determine the energy resolution.

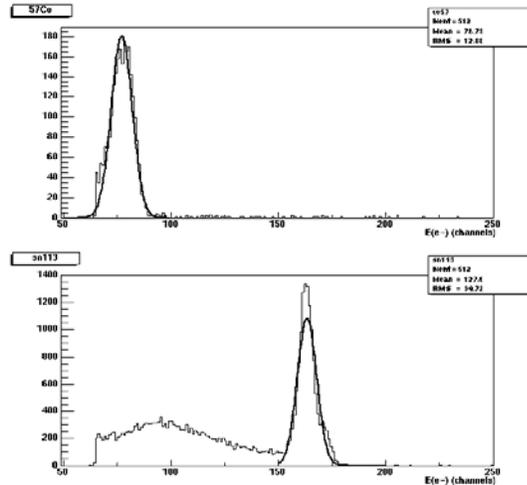
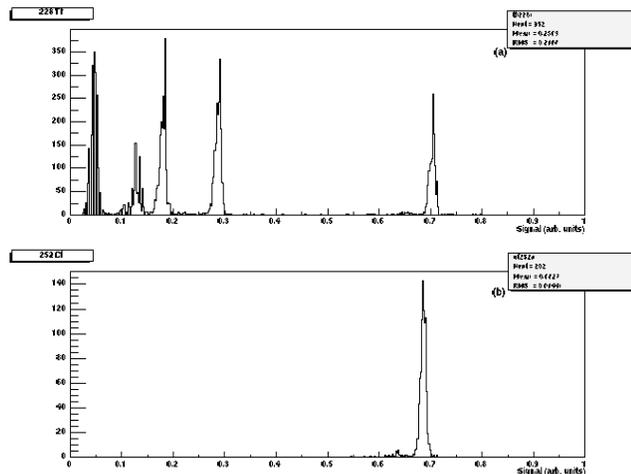


Figure 3 illustrates the performance attainable for alpha particles from (a) a  $^{228}\text{Th}$  source with several alpha-particle energies, with the readout directly connected to a single pad of the detector, and (b) a  $^{252}\text{Cf}$  source. In the latter case the readout was done through the multiplexed output of the chip, and was triggered using a NaI(Tl) detector that was used to detect the coincident 100.2 keV gamma that accompanies the 5.977 MeV alpha particle. In both cases, the observed alpha particle energy resolution is between 30 and 40 keV, well within the requirements of typical charged-particle spectroscopy requirements.

Figure 3. Alpha-particle energy spectra measured with a silicon pad detector read out with the VA-HDR2 chip. (a) Partial spectrum of alpha particles from a  $^{228}\text{Th}$  source for a single pad of the detector, where the VA-HDR chip multiplex readout was bypassed and signals were taken only from a single pad. (b) Spectrum of alpha particles from  $^{252}\text{Cf}$ , where the readout of the HDR chip was triggered with a NaI detector.



Latchup and radiation-induced single-event-upsets (SEU). There exists substantial evidence that the technology used in the chip fabrication, namely CMOS, can be sensitive to single-event-upset (SEU) problems caused by ionizing radiation incident directly on the readout chip. Briefly, the production of charge in certain regions of the readout chip may create parasitic transistor structures linking, in the worse case, the affected regions of the chip with the bulk silicon substrate. Under certain conditions, these parasitic transistors can conduct large currents between the supply voltages and ground. In some cases, these currents may be large enough to fuse or melt the small bond wires that connect the chip to the hybrid PC board upon which it is mounted. We

have investigated the effects of ionizing radiation on the VA-HDR chips in a typical low-energy, heavy-ion scattering environment.

The experiment was carried out using a 400 MeV  $^{86}\text{Kr}$  beam from ATLAS. The  $^{86}\text{Kr}$  ions were scattered from a  $100\text{-}\mu\text{g}/\text{cm}^2$  Au foil, onto one pad-detector plus chip module. The scattered Kr ions were collimated such that particles could strike only a selected set of silicon pads, or the VA-HDR chip itself. In order to provide a trigger for the VA-HDR readout, the ions first traversed a thin silicon surface-barrier  $\Delta E$  detector. Two pad detectors were evaluated. CMOS latchup induced by the Kr irradiation was observed to occur in both. In each case, the ion that caused the latchup was directly incident on the VA-HDR chip itself, not the silicon sensor. This result suggests that the CMOS latchup problem is truly due to ionizing radiation inducing clouds of unwanted charge in the chip, and not to large signals at the input stages of the chip. The physical effects of this bombardment are illustrated in Fig. 4, which shows a photograph of thin-wire bonds attached to the power-supply area of one affected chip. The +2V power supply bond has been fused in the latchup event, as shown. From these tests, it is clear that any design incorporating these chips as front-end readout devices should endeavor to protect the chips from direct charged-particle irradiation. We do emphasize, however, that in the cases where the currents drawn are large enough to melt the bond wires, the damaging effects of the latchup are terminated, and little residual damage to the chip itself is sustained. In fact, if the fused bonding connections are repaired, the chip recovers its earlier performance.

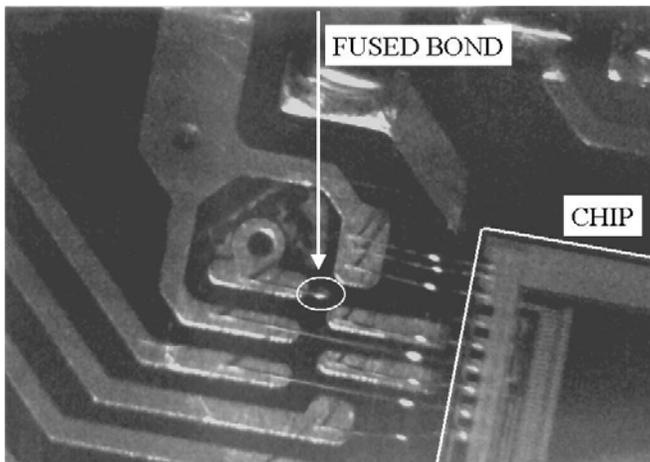


Figure 4. Photograph of a damaged bond wire that was melted in a CMOS latchup event.

Planar Germanium Wafers. In addition to R&D in large area, high granularity, silicon detectors we have begun research into developing large area, position-sensitive, planar germanium wafers. The wafers are physically much larger than current silicon detectors, especially in thickness. Whereas silicon detectors are usually  $< 1\text{mm}$  thick, germanium counters can be  $> 20\text{mm}$ . These detectors will be useful for detection of high-energy particles, but, more importantly, for detecting  $\gamma$  rays. We have worked with ORTEC, the

premier U.S. germanium detector manufacturer, to develop the world's largest germanium wafers, 90mm x 90mm x 20mm. As with silicon, first level position sensitivity is achieved by sub-dividing the electrodes into orthogonal strips. In the present detector, these electrodes are 5mm wide, giving a 16 x 16 strip detector with 256 pixels. Each strip will have excellent energy resolution (<800 eV at 122 keV, <1.7 keV at 1.33 MeV), timing (FWHM <5ns for  $\gamma$  rays >122 keV) and high count rate capability (>50,000/strip/sec). We are testing our second device, which is approaching these goals.

We have been investigating sub-strip resolution through measuring the image charges created when particles interact with germanium. For the case of  $\gamma$ -ray detection, the particles are electrons generated by the photoelectric effect, or by Compton scattering. The charge drift time in the germanium wafer is hundreds of nanoseconds, and during that time neighboring strips experience induced transients, which depend on the location of the primary charge. Using digital pulse processing we have captured many of these images and are developing algorithms to locate the interactions. Even simple algorithms seem to provide 1/10 sub-strip reconstruction, i.e., 0.5 mm, while the charge pulse rise time gives depth information at the 1mm level. Thus, it appears that a  $\gamma$ -ray detector with superior spatial, timing and energy resolution is achievable in the very near future.

To take advantage of the image charge reconstruction, high density, low cost (~\$500/channel), high-bandwidth (>100 mega samples/sec), digital data processing is vital. We are involved in developing such electronics

**Specific Accomplishments:** No publications on this work have yet appeared.